

Figure 1 - FPGA blocks for User-specific functions and I/O interfaces

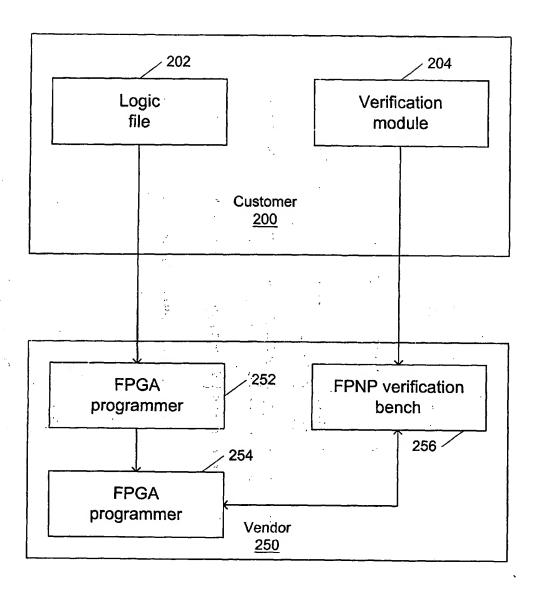


Fig. 2

RPS920010125US1
C. E. Kuhlmann et al.
Field Programmable Network Processor and Method for Customizing a Network Processor

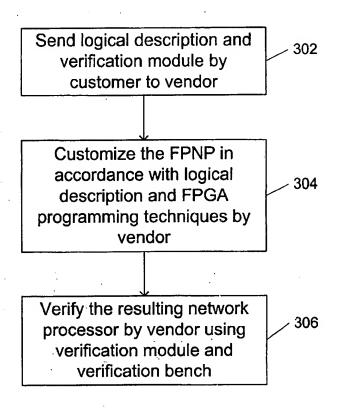


Fig. 3